DATA SHEET

SC26C562

CMOS dual universal serial communications controller (CDUSCC)

Product data sheet
Supersedes data of 2004 Mar 29

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Philips
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CMOS dual universal serial communications controller (CDUSCC) SC26C562

DESCRIPTION

The Philips Semiconductors SC26C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC26C562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC26C562 (CDUSCC) is (PIN) hardware and (REGISTER) software compatible with the existing SCN26562 (DUSCC). CDUSCC will automatically configure to the NMOS DUSCC register map (default mode) on power-up.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the CDUSCC well-suited for dual-speed channel applications. Data rates up to 10 Mbit/s are supported.

The transmitter and receiver each contain a sixteen-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

The SC26C562 CDUSCC is optimized to interface with processors using a synchronous bus interface, such as the 8086, and iAPX86 family. For systems using an asynchronous bus, such as the 68000 and 68010, refer to the SC68C562 documentation.

Refer to the CMOS Dual Universal Serial Communication Controller (CDUSCC) User's Manual for a complete operational description.

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: Single SYNC, dual SYNC, BiSYNC, DDCMP
  - ASYNC: 5-8 bits plus optional parity
- Sixteen character receive and transmit FIFOs with interrupt threshold control
- FIFO'ed status bits
- Watchdog timer
- 0 to 10 Mbit/s data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64 kbaud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Synchronous and Asynchronous bus DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/ timer terminal count or DMA DONE (EOPN)
- Transmit path clear status
- High speed data bus interface: 160 ns bus cycle
- DPLL operation up to 312.5 kHz with internal clock
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Individual interrupt enable bits
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 80XX/X compatible
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5 V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun and framing error detection
- False start bit detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit and receive up to 10 Mbit/s at 1× or 1 Mbit/s at 16× data rates

Bit-Oriented Protocol

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Transmit 7 or 8 bit ABORT
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

Character-Oriented Protocols

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill or underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun and underrun error detection
- Optional SYNC exclusion from FCS
- BISYNC features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text
  - Parity generation for data and LRC characters

ORDERING INFORMATION

T_{amb} = 0 °C to +70 °C. Serial data rate = 10 Mbit/s maximum

Type number	Package		
	Name	Description	Version
SC26C562C1A	PLCC52	plastic leaded chip carrier; 52 leads	SOT238-2

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_{amb}	Operating ambient temperature[2]	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V

BLOCK DIAGRAM

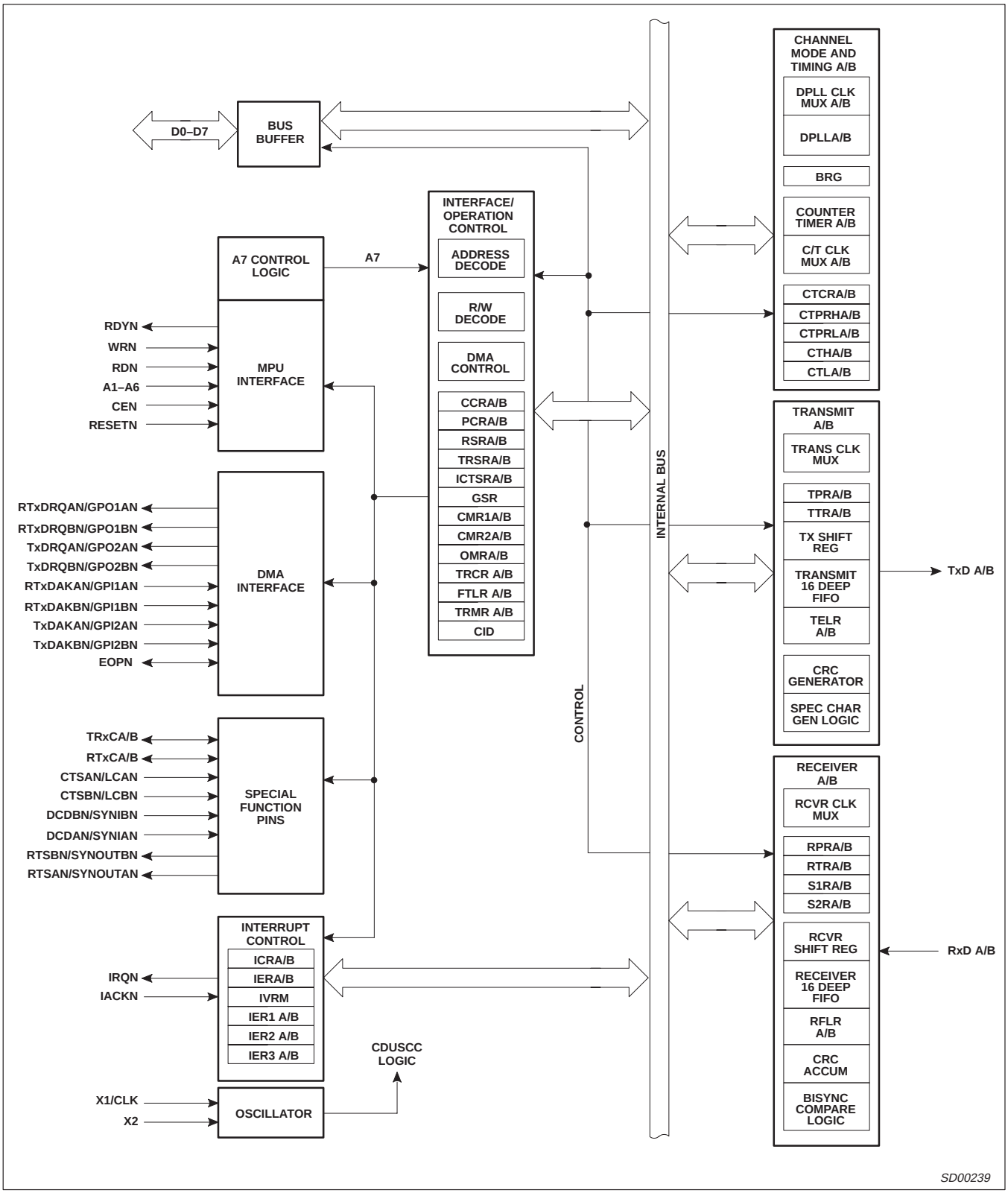
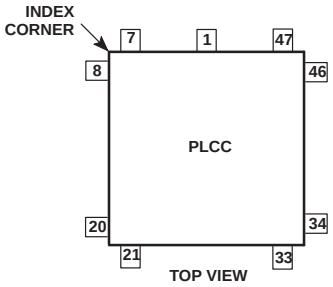


Figure 1. Block diagram

PIN CONFIGURATION



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/GPI1BN	31	D2
6	IRQN	32	D1
7	NC	33	D0
8	RDYN	34	NC
9	RTSBN/SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/GPO1AN
12	DCDBN/SYNIBN	38	TxDAKAN/GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/GPI2BN	42	DCDAN/SYNIAN
17	RTxDRQBN/GPO1BN	43	RTxCA
18	TxDRQBN/GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/SYNOUTAN
20	D7	46	X2
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/GPI1AN
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	V_{CC}

SD00740

Figure 2. Pin configuration

PIN DESCRIPTION

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
A1–A6	4-2, 51-49	I	**Address Lines:** Active-HIGH. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-HIGH, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and RDN, or CSN and WRRN are LOW during interrupt acknowledge cycles and single address DMA acknowledge cycles.
RDN	24	I	**Read Strobe:** Active-LOW input. When active and CSN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CSN is active.
WRN	28	I	**Write Strobe:** Active-LOW input. When active and CSN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CSN	27	I	**Chip Select:** Active-LOW input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by RDN or WRN and A1–A6 inputs. When CSN is HIGH, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
RDYN	8	O	**Ready:** Active-LOW, open drain. Used to synchronize data transfers between the CPU and the CDUSCC. It is valid only during read and write cycles where the CDUSCC is configured in ‘wait on Rx’, ‘wait on Tx’ or ‘wait on Tx or Rx’ modes, otherwise it is always inactive. RDYN becomes active on the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
IRQN	6	O	**Interrupt Request:** Active-LOW, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-LOW. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	46	O	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin should be left floating.
RESETN	25	I	**Master Reset:** Active-LOW. A LOW on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (HIGH) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).
CTSA/BN, LCA/BN	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-LOW. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-LOW input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-LOW external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-LOW. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-LOW. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-LOW. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.

MNEMONIC	PIN	TYPE	NAME AND FUNCTION
TxDAKA/BN, GPI2A/BN	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-LOW. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
EOPN	29	I/O	**Done (EOP):** Active-LOW, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. As an input, EOPN indicates the last DMA transfer cycle to the TxFIFO. As an output, EOPN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-LOW. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{CC}	34, 52	I	**+5 V Power Input**
GND	26, 13, 41, 7	I	**Signal and Power Ground Input**

DC ELECTRICAL CHARACTERISTICS[4,5]

T_{amb} = 0 °C to +70 °C, V_{CC} = 5.0 V ± 10 %[4,5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input LOW voltage: All except X1/CLK X1/CLK		 – –	 – –	 0.8 0.8	 V V
V_{IH}	Input HIGH voltage except X1/CLK All except X1/CLK X1/CLK		 2.0 $0.8 \times V_{CC}$	 – –	 – V_{CC}	 V V
V_{OL}	Output LOW voltage: All except IRQN[7] IRQN	 I_{OL} = 5.3 mA I_{OL} = 8.8 mA	 – –	 – –	 – 0.5	 V V
V_{OH}	Output HIGH voltage (Except open drain outputs)	I_{OH} = –400 µA	V_{CC} – 0.5	–	0.5	V
I_{ILX1}	X1/CLK input LOW current[10]	V_{IN} = 0, X2 = open	–150	–	0.0	µA
I_{IHX1}	X1/CLK input HIGH current[10]	$V_{IN} = V_{CC}$, X2 = GND	–	–	150	µA
I_{SCX2}	X2 short circuit current	X1 = open, V_{IN} = 0 V	–	–	–15	mA
		X1 = open, $V_{IN} = V_{CC}$	–	–	+15	mA
I_{IL}	Input LOW current RESETN, TxDAKN, RxDAKN	V_{IN} = 0 V	–15	–	–0.5	µA
I_I	Input leakage current	V_{IN} = 0 V to V_{CC}	–1	–	+1	µA
I_{OZH}	Output off current HIGH, 3-State data bus	$V_{IN} = V_{CC}$	–	–	+1	µA
I_{OZL}	Output off current LOW, 3-State data bus	V_{IN} = 0 V	–1	–	–	µA
I_{ODL}	Open drain output LOW current in off state: EOPN, RDYN IRQN	 V_{IN} = 0 V V_{IN} = 0 V	 –15 –1	 – –	 –0.5 –	 µA µA
I_{ODH}	Open drain output HIGH current in off state: EOPN, IRQN, RDYN	 $V_{IN} = V_{CC}$	 –1	 –	 1	 µA
I_{CC}[13]	Power supply current (see Figure 19 for graphs)		–	25	80	mA
C_{IN}	Input capacitance[9]	V_{CC} = GND = 0 V	–	–	10	pF
C_{OUT}	Output capacitance[9]	V_{CC} = GND = 0 V	–	–	15	pF
$C_{I/O}$	Input/output capacitance[9]	V_{CC} = GND = 0 V	–	–	20	pF

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. Clock may be stopped (DC) for testing purposes, or when CDUSCC is in non-operational modes.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.2 V and 3.0 V with a transition time of 20 ns maximum. For X1/CLK, this swing is between 0.2 V and 4.4 V. All time measurements are referenced at input voltages of 0.2 V and 3.0 V and output voltages of 0.8 V and 2.0 V, as appropriate.
6. See Figure 20 for test conditions for outputs.
7. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2 V above the actual output signal level. This point represents noise margin that assures true switching has occurred.
8. Execution of the valid command (after it is latched) requires 3 rising edges of X1 (see Figure 15).
9. These values were not explicitly tested; they are guaranteed by design and characterization data.
10. X1/CLK and X2 are not tested with a crystal installed.
11. X1/CLK frequency must be at least the faster of the receiver or transmitter serial data rate.
12. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CSN as the ‘strobing’ input. CSN and RDN (also CSN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
13. V_O = 0 V to V_{CC}, Rx and Tx clocks at 10 MHz, X1 clock at 10 MHz.

AC ELECTRICAL CHARACTERISTICS[4,5,6,7]

T_{amb} = 0 °C to +70 °C; V_{CC} = 5 V ± 10 %

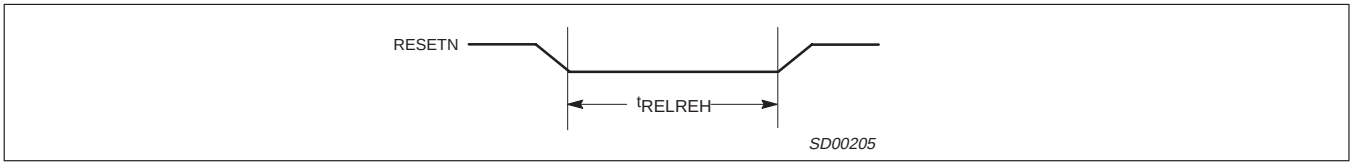


Figure 3. Reset Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RELREH}	RESETN LOW to RESETN HIGH	200	–	ns

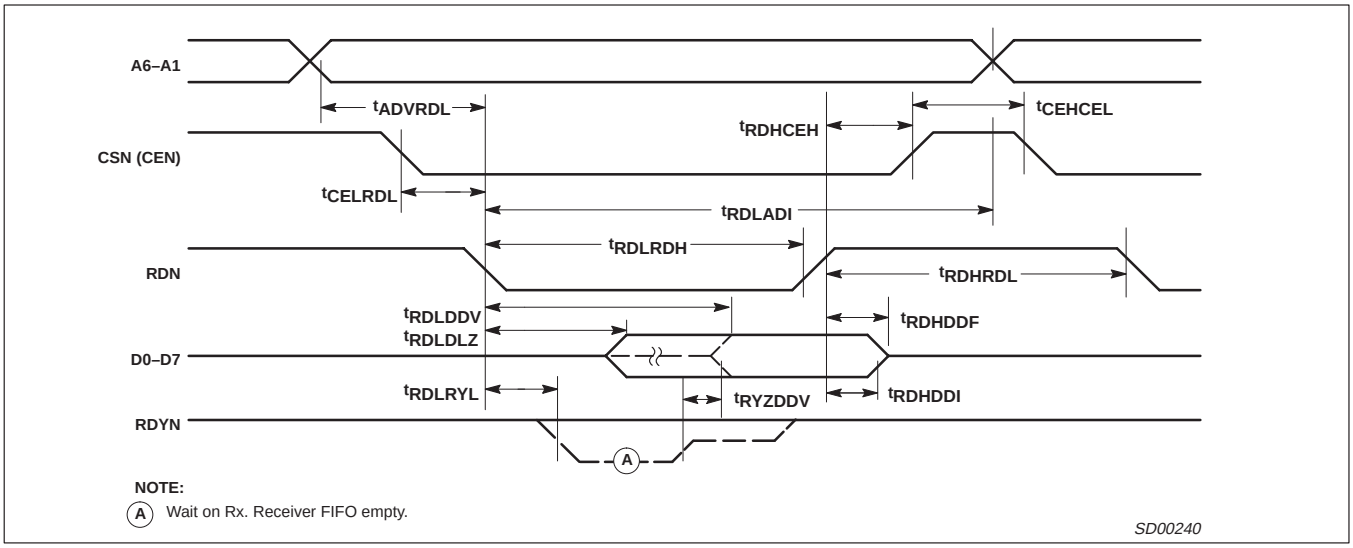


Figure 4. Read Cycle[12]

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{ADVRDL}	Address valid to RDN LOW	5	–	ns
t_{CELRDL}	CEN LOW to RDN LOW	0	–	ns
t_{RDLADI}	RDN LOW to address invalid	50	–	ns
t_{RDLRYL}	RDN LOW to RDYN LOW	–	150	ns
t_{RDLDDV}	RDN LOW to read data valid	–	130	ns
t_{RDLRDH}	RDN LOW to RDN HIGH	130	–	ns
t_{RYZDDV}	RDYN high-impedance to read data valid[9]	–	90	ns
t_{RDHCEH}	RDN HIGH to CEN HIGH	0	–	ns
t_{CEHCEL}	CEN HIGH to CEN LOW	30	–	ns
t_{RDHDDI}	RDN HIGH to read data invalid	5	–	ns
t_{RDHRDL}	RDN HIGH to RDN LOW	30	–	ns
t_{RDHDDF}	RDN HIGH to data bus floating	–	40	ns
t_{RDLDLZ}	RDN LOW to data bus low-impedance[9]	10	–	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

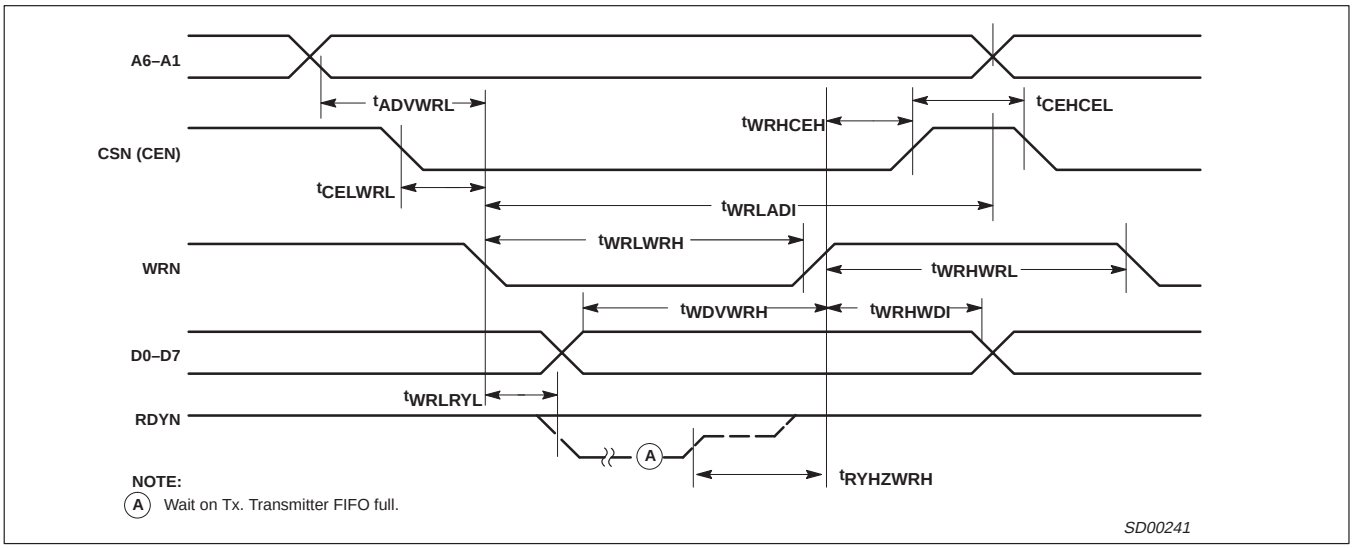


Figure 5. Write Cycle[12]

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{ADVWRL}	Address valid to WRN LOW	5	–	ns
t_{CELWRL}	CSN LOW to WRN LOW	0	–	ns
t_{WRLRYL}	WRN LOW to RDYN LOW	–	–	ns
t_{WRHCEH}	WRN HIGH to CSN HIGH	0	–	ns
t_{WRLWRH}	WRN LOW to WRN HIGH	100	–	ns
t_{WDVWRH}	Write data valid to WRN HIGH	60	–	ns
t_{CEHCEL}	CEN HIGH to CEN LOW	30	150	ns
t_{WRLADI}	WRN LOW to address invalid	50	–	ns
t_{WRHWRL}	WRN HIGH to WRN LOW	30	–	ns
t_{WRHWDI}	WRN HIGH to write data invalid	5	–	ns
$t_{RYHZWRH}$	RDYN high-impedance to WRN HIGH[9]	0	–	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

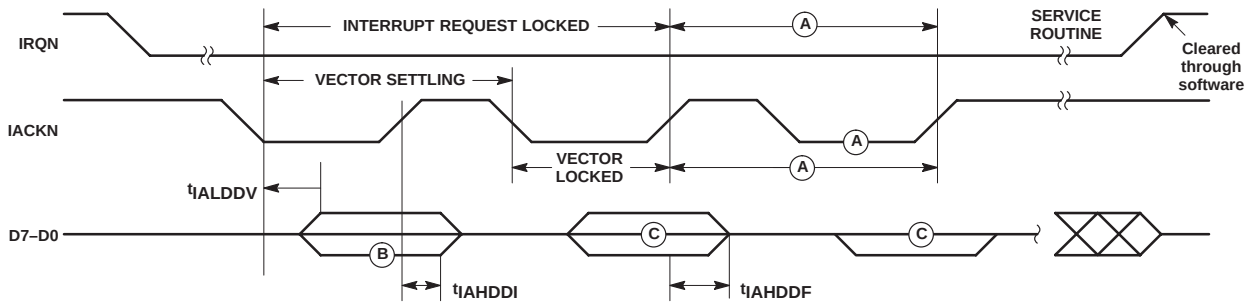


Figure 6. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{IALDDV}	IACKN LOW to data bus valid			ns
t_{IAHDDF}	IACKN HIGH to data bus floating		130	ns
t_{IAHDDI}	IACKN HIGH to data bus invalid	5	60	ns
t_{IALDLZ}	IACKN LOW to data bus LOW impedance[9]	10		ns
t_{IAHIAL}	IACKN HIGH to LOW	30		ns

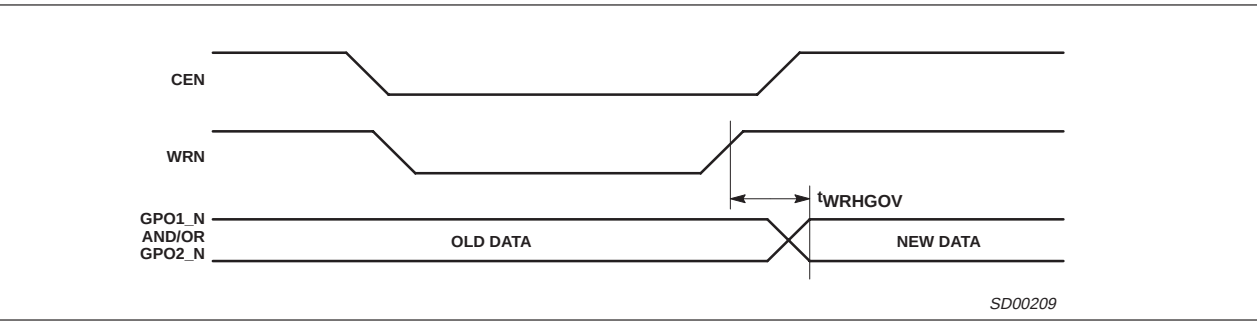


Figure 7. Output Port Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{WRHGOV}	WRN HIGH to GPO output data valid	–	100	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

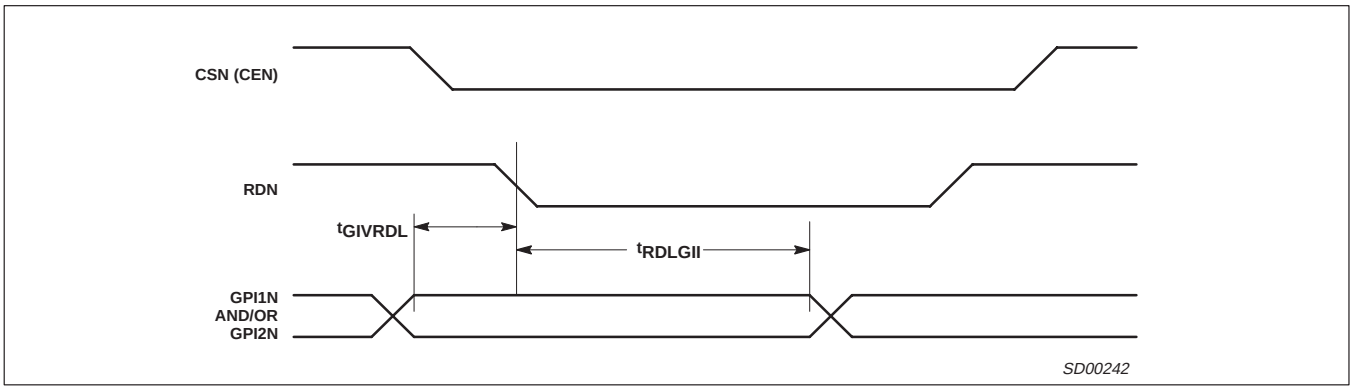


Figure 8. Input Port Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{GIVRDL}	GPI input valid to RDN LOW	20	–	ns
t_{RDLGII}	RDN LOW to GPI input invalid	40	–	ns

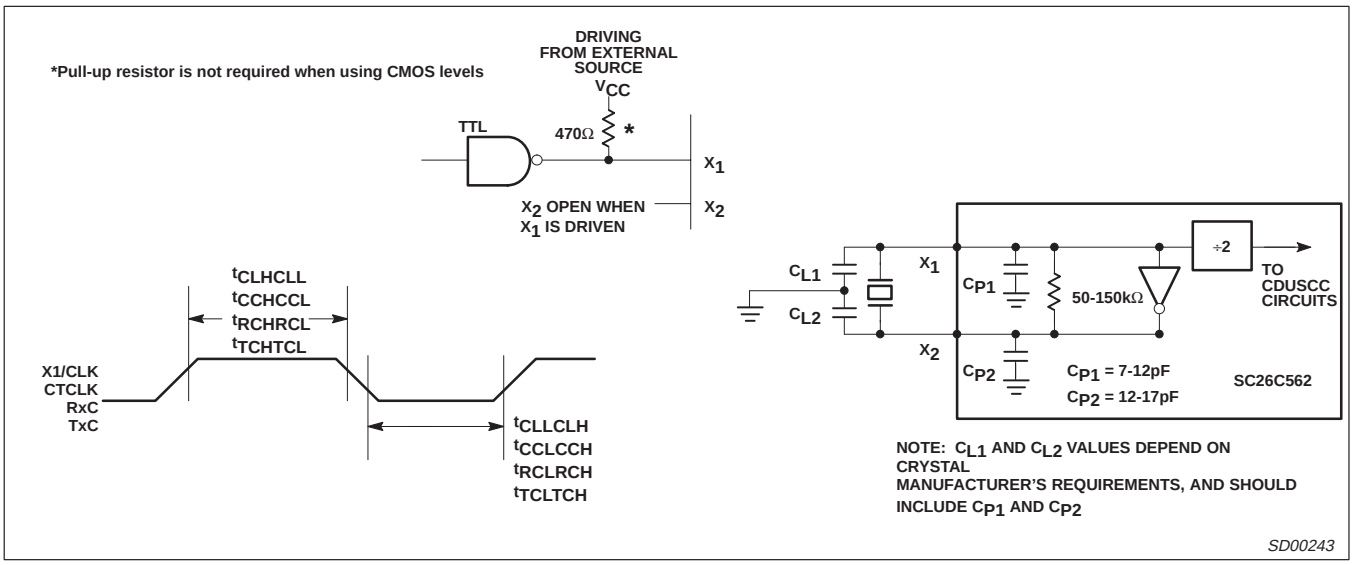


Figure 9. Clock Timing

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{CLHCLL}	X1/CLK HIGH to LOW time	25	–	–	ns
t_{CLLCLH}	X1/CLK LOW to HIGH time	25	–	–	ns
t_{CCHCCL}	C/T CLK HIGH to LOW time	45	–	–	ns
t_{CCLCCH}	C/T CLK LOW to HIGH time	45	–	–	ns
t_{RCHRCL}	RxC HIGH to LOW time	50	–	–	ns
t_{RCLRCH}	RxC LOW to HIGH time	50	–	–	ns
t_{TCHTCL}	TxC HIGH to LOW time	50	–	–	ns
t_{TCLTCH}	TxC LOW to HIGH time	50	–	–	ns
f_{CL}	X1/CLK frequency[11]	0	14.7456	16.0	MHz
f_{CC}	C/T CLK frequency	0	–	10	MHz
f_{RC}	RxC frequency (16X or 1X @ 50% duty cycle)	0	–	10	MHz
f_{TC}	TxC frequency (16X or 1X @ 50% duty cycle)	0	–	10	MHz
f_{RTC}	Tx/Rx frequency for FM/Manchester encoding	–	–	5	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

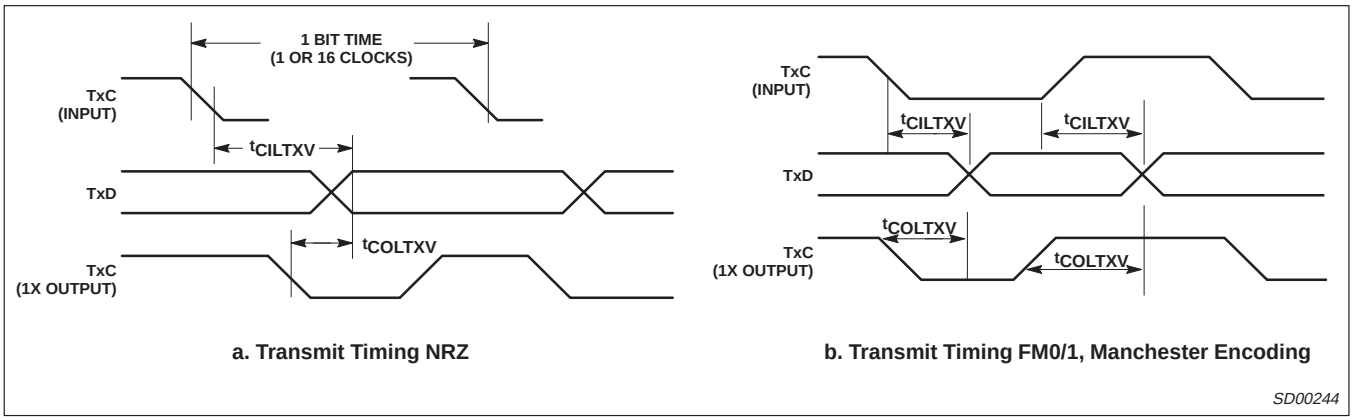


Figure 10.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{CILTXV}	TxC input LOW (1X) to TxD output	–	120	ns
	TxC input LOW (16X) to TxD output	–	120	ns
t_{COLTXV}*	TxC output LOW to TxD output[9] (NRZ, NRZI)	–	20	ns
	FM, MAN	–	30	ns
*Characterized with no loads on TxD and TxC outputs. Tester load is approximately 50 pF.				

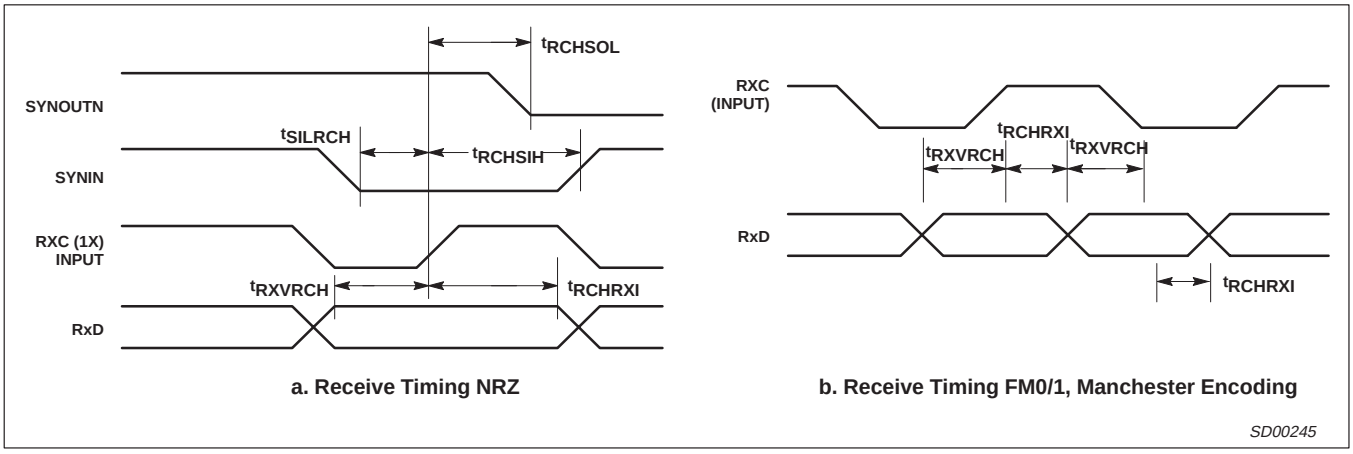


Figure 11.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RXVRCH}	RxD data valid to RxC HIGH:			
	For NRZ data	20	–	ns
	For NRZI, Manchester, FM0, FM1 data	30	–	ns
t_{RCHRXI}	RxC HIGH to RxD data invalid:			
	For NRZ data	20	–	ns
	For NRZI, Manchester, FM0, FM1 data	30	–	ns
t_{SILRCH}	SYNIN LOW to RxC HIGH	50	–	ns
t_{RCHSIH}	RxC HIGH to SYNIN HIGH	20	–	ns
t_{RCHSOL}	RxC HIGH to SYNOUT LOW	–	100	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

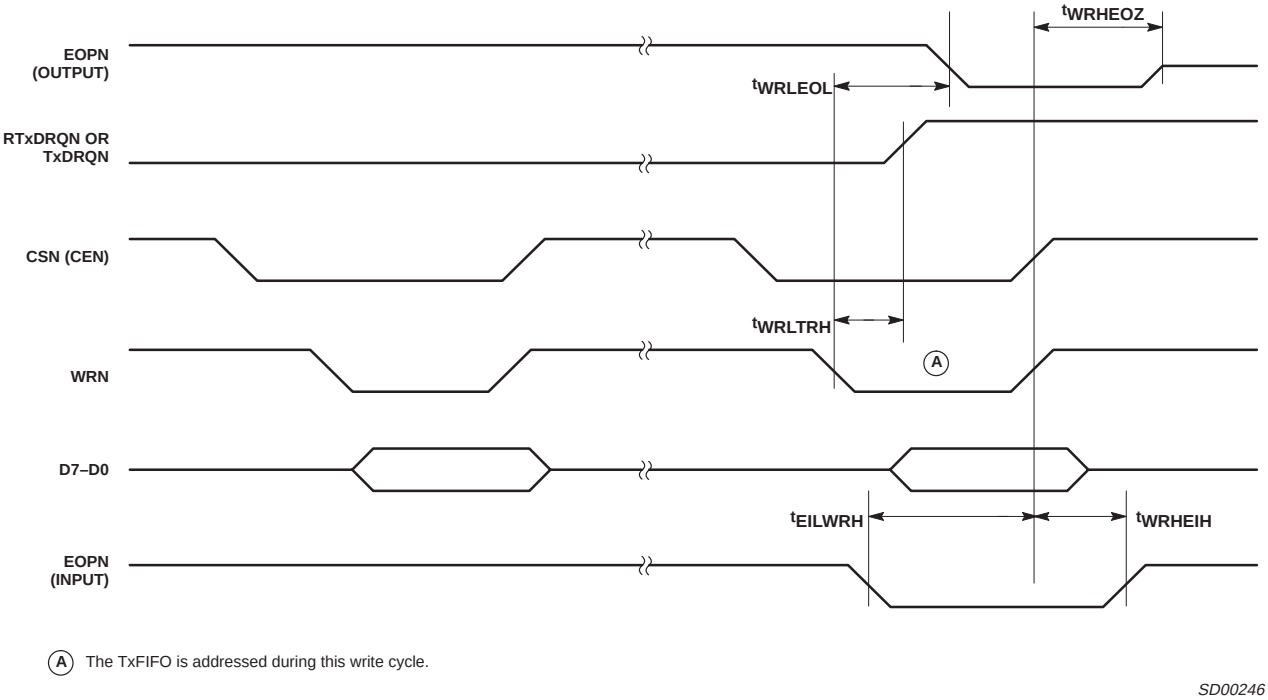


Figure 12. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{WRLTRH}	WRN LOW to Tx DMA REQN HIGH	–	100	ns
t_{WRLEOL}	WRN LOW to EOPN output LOW	–	100	ns
t_{WRHEOZ}	WRN HIGH to EOPN output high-impedance	–	60	ns
t_{EILWRH}	EOPN input LOW to WRN HIGH	30	–	ns
t_{WRHEIH}	WRN HIGH to EOPN input HIGH	25	–	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

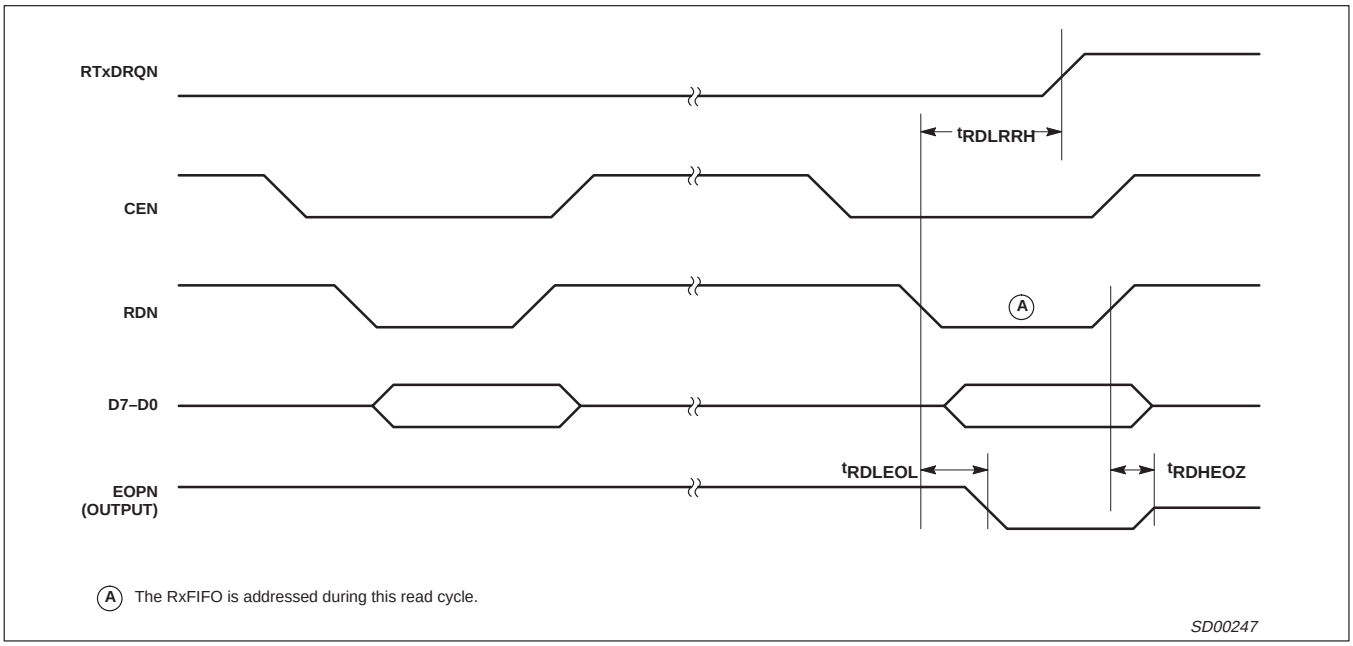


Figure 13. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RDLRRH}	RDN LOW to Rx DMA REQN HIGH	–	100	ns
t_{RDLEOL}	RDN LOW to EOPN output LOW	–	100	ns
t_{RDHEOZ}	RDN HIGH to EOPN output high-impedance	–	60	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

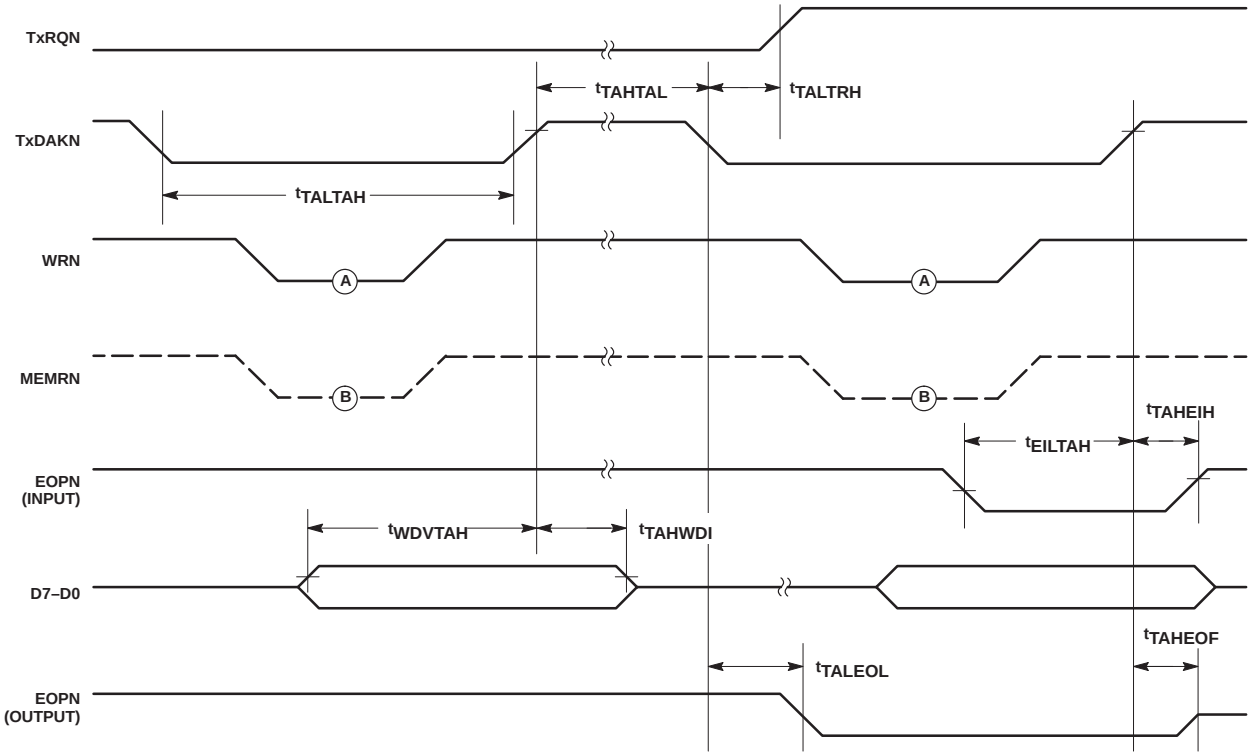


Figure 14. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{TAHTAL}	Transmit DMA ACKN HIGH to LOW time	30	–	ns
t_{TALTAH}	Transmit DMA ACKN LOW to HIGH time	100	–	ns
t_{TALTRH}	Tx DMA ACKN LOW to Tx DMA REQN HIGH	–	100	ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN HIGH	40	–	ns
t_{TAHWDI}	Tx DMA ACKN HIGH to write data invalid	10	–	ns
t_{TALEOL}	Tx DMA ACKN LOW to EOPN output LOW	–	80	ns
t_{TAHEOF}	Tx DMA ACKN HIGH to EOPN output float	–	60	ns
t_{EILTAH}	EOPN input LOW to Tx DMA ACKN HIGH	30	–	ns
t_{TAHEIH}	Tx DMA ACKN HIGH to EOPN input HIGH	25	–	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

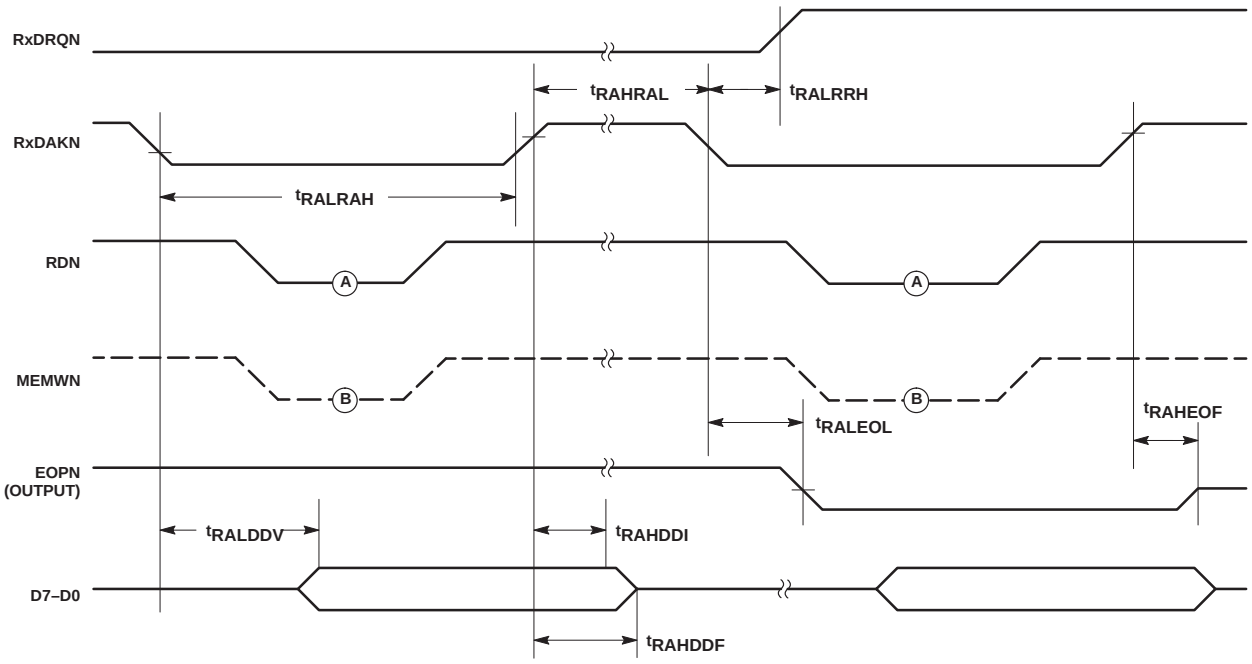


Figure 15. DMA-Receive Single Address Mode

SYMBOL		LIMITS		UNIT
		Min	Max	
t_{RAHRAL}	Receive DMA ACKN HIGH to LOW time	30	–	ns
t_{RALRAH}	Receive DMA ACKN LOW to HIGH time	130	–	ns
t_{RALRRH}	Rx DMA ACKN LOW to Rx DMA REQN HIGH	–	100	ns
t_{RALEOL}	Rx DMA ACKN LOW to EOPN output LOW	–	100	ns
t_{RAHEOF}	Rx DMA ACKN HIGH to EOPN output float	–	60	ns
t_{RALDDV}	Rx DMA ACKN LOW to read data valid	–	130	ns
t_{RAHDDI}	Rx DMA ACKN HIGH to read data invalid	5	–	ns
t_{RAHDDF}	Rx DMA ACKN HIGH to data bus float	–	60	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

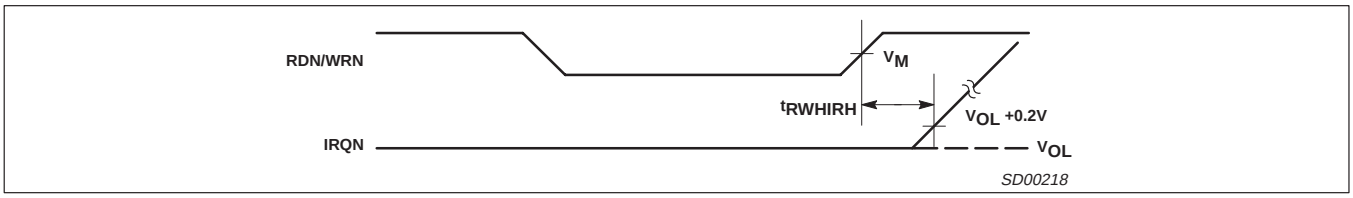


Figure 16. Interrupt Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RWHIRH}	RDN/WRN HIGH to IRQN HIGH for:			
	Read RxFIFO (RxRDY interrupt)	–	90	ns
	Write TxFIFO (TxRDY interrupt)	–	90	ns
	Write RSR (Rx condition interrupt)	–	90	ns
	Write TRSR (Rx/Tx interrupt)	–	90	ns
	Write ICTSR (counter/timer interrupt)	–	90	ns
	Write TRMSR (Tx Path, Patt. Det.)	–	90	ns

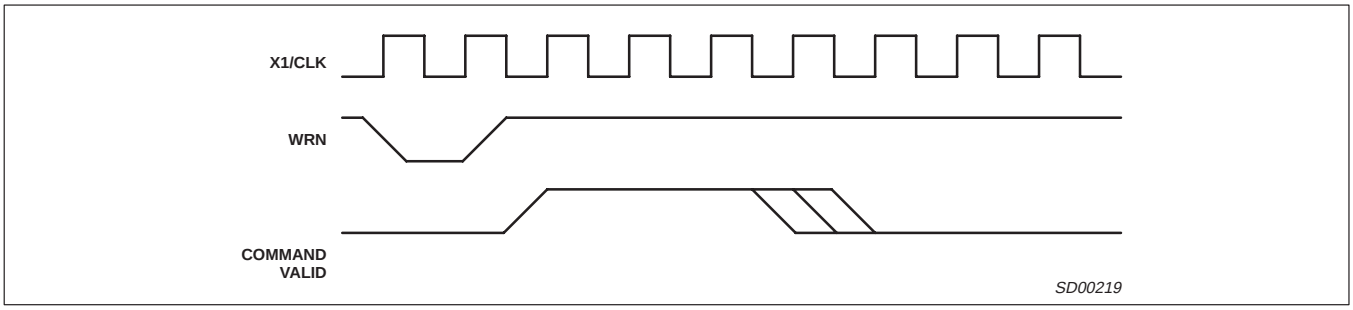


Figure 17. Command Timing

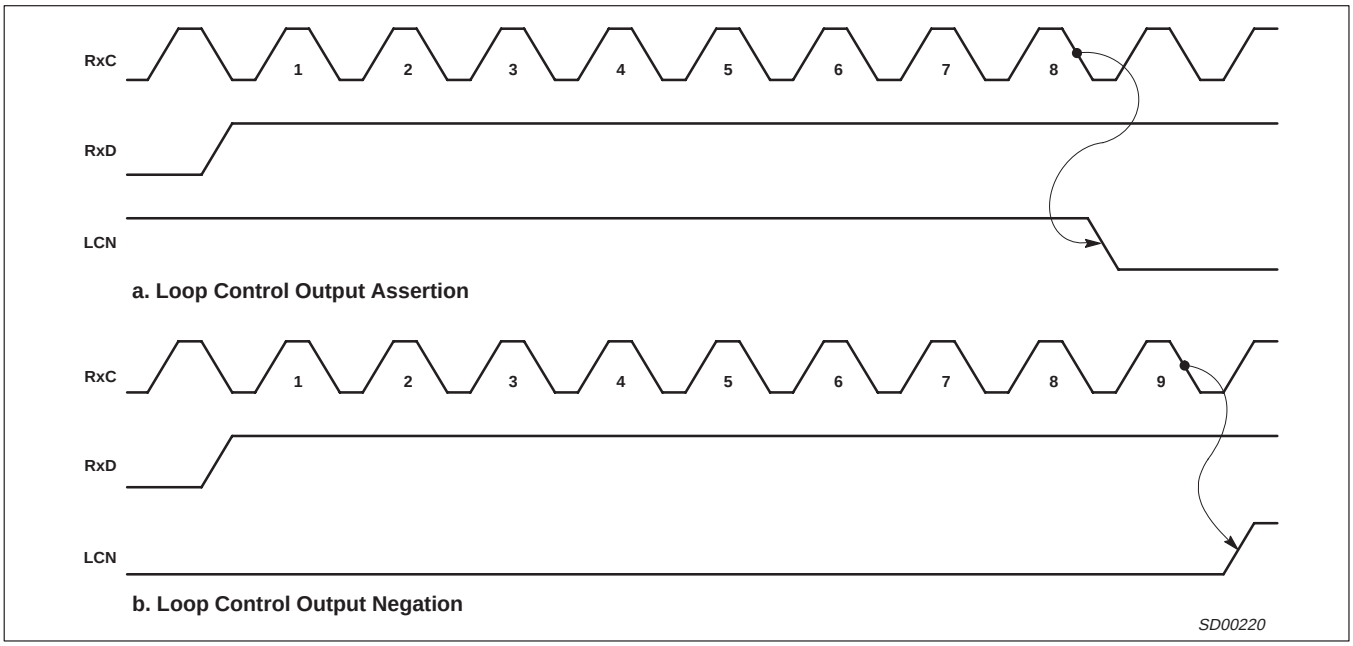


Figure 18. Relationship Between Received Data and the Loop Control Output

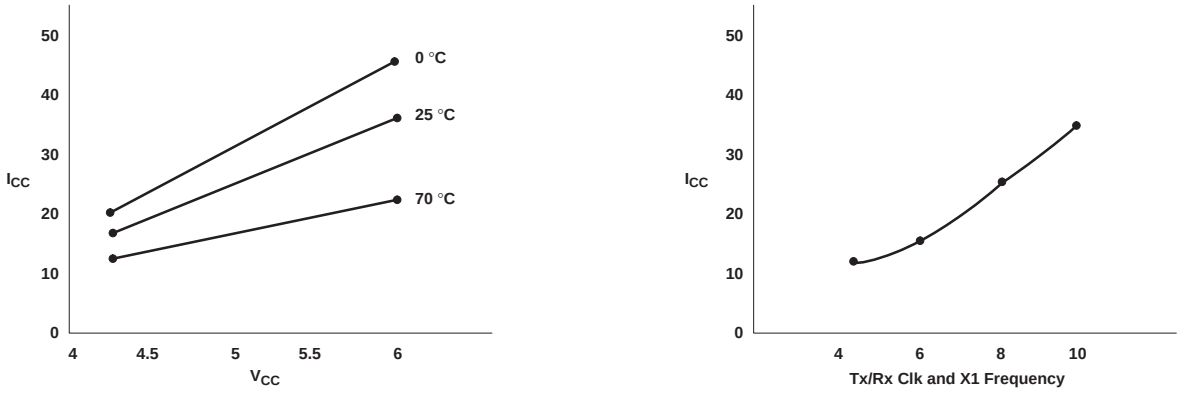


Figure 19.

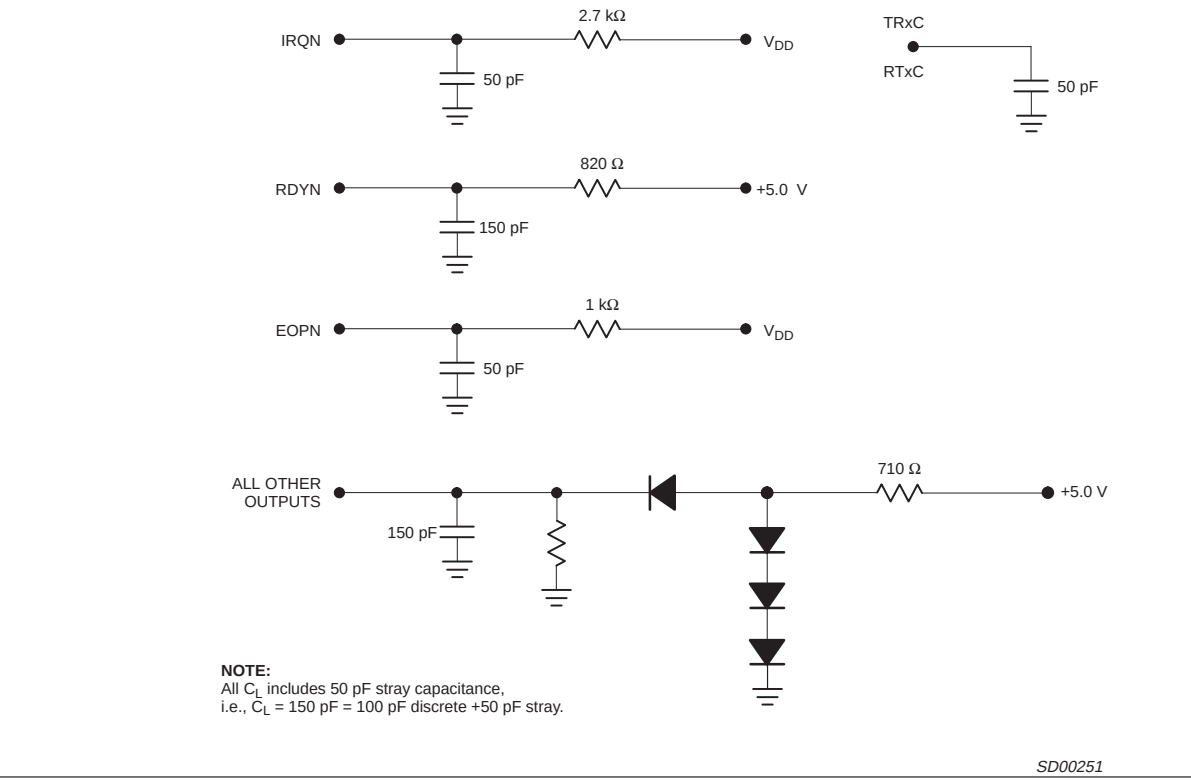
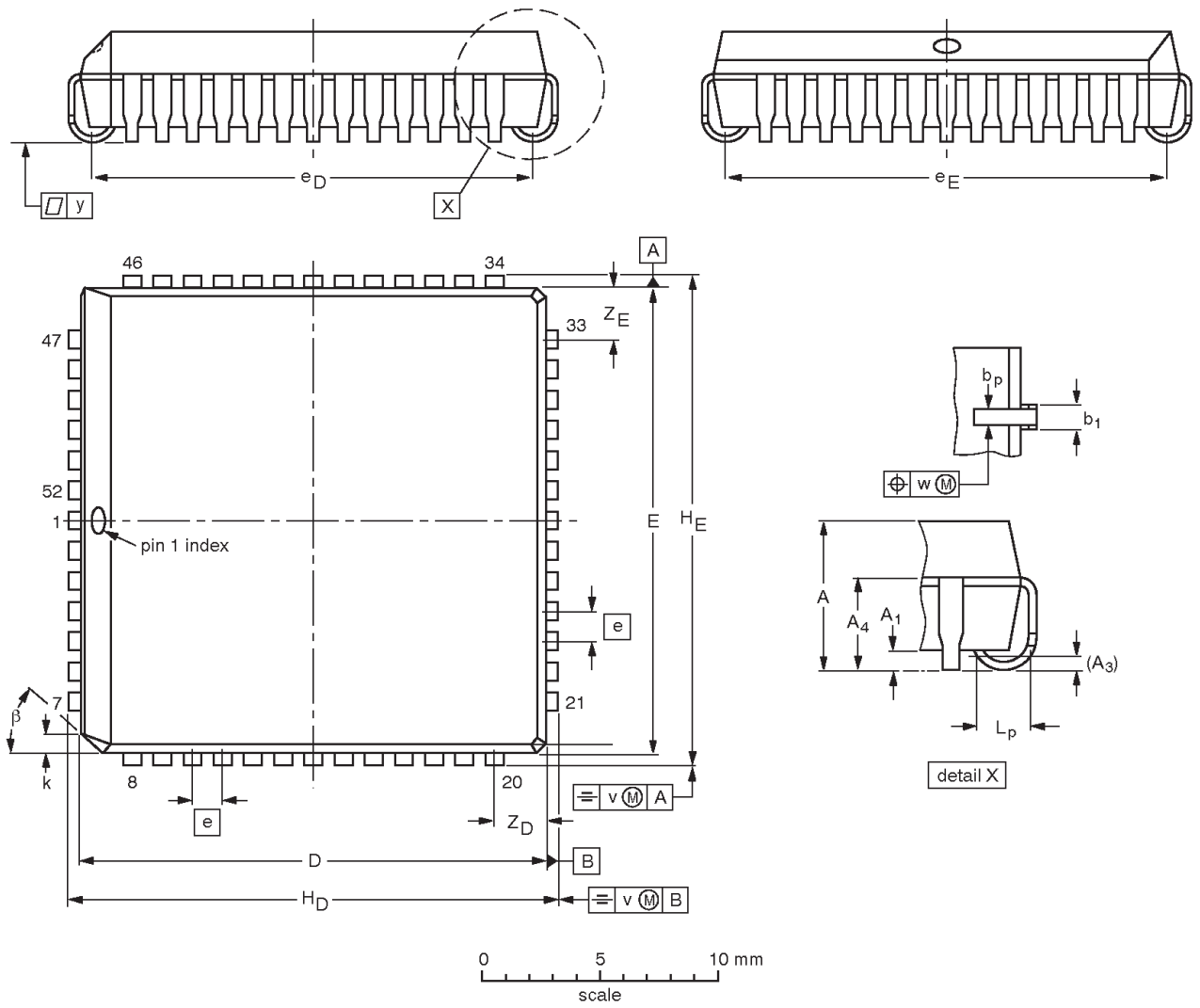


Figure 20. Test Conditions for Outputs

PLCC52: plastic leaded chip carrier; 52 leads **SOT238-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	19.20 19.05	19.20 19.05	1.27	18.54 17.53	18.54 17.53	20.19 19.94	20.19 19.94	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.756 0.750	0.756 0.750	0.05	0.73 0.69	0.73 0.69	0.795 0.785	0.795 0.785	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT238-2	112E11	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

REVISION HISTORY

Rev	Date	Description
_4	20060810	**Product data sheet (9397 750 14948). Supersedes data of 2004 Mar 29 (9397 750 13072).** Modifications: ● Ordering information: changed Version for PLCC52 from SOT238–3 to SOT238–2 ● Changed package outline drawing from SOT238–3 to SOT238–2.
_3	20040329	**Product data (9397 750 13072). Supersedes Product specification of 1998 Sep 04 (9397 750 04355).**
_2	19980904	**Product specification (9397 750 04355). ECN 853-1663 19973 of 04 September 1998. Supersedes data of 1995 May 01.**
_1	19950501	

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